Responding to Dynamic Workloads and Varying Harvested Energy in Energy Constrained Systems

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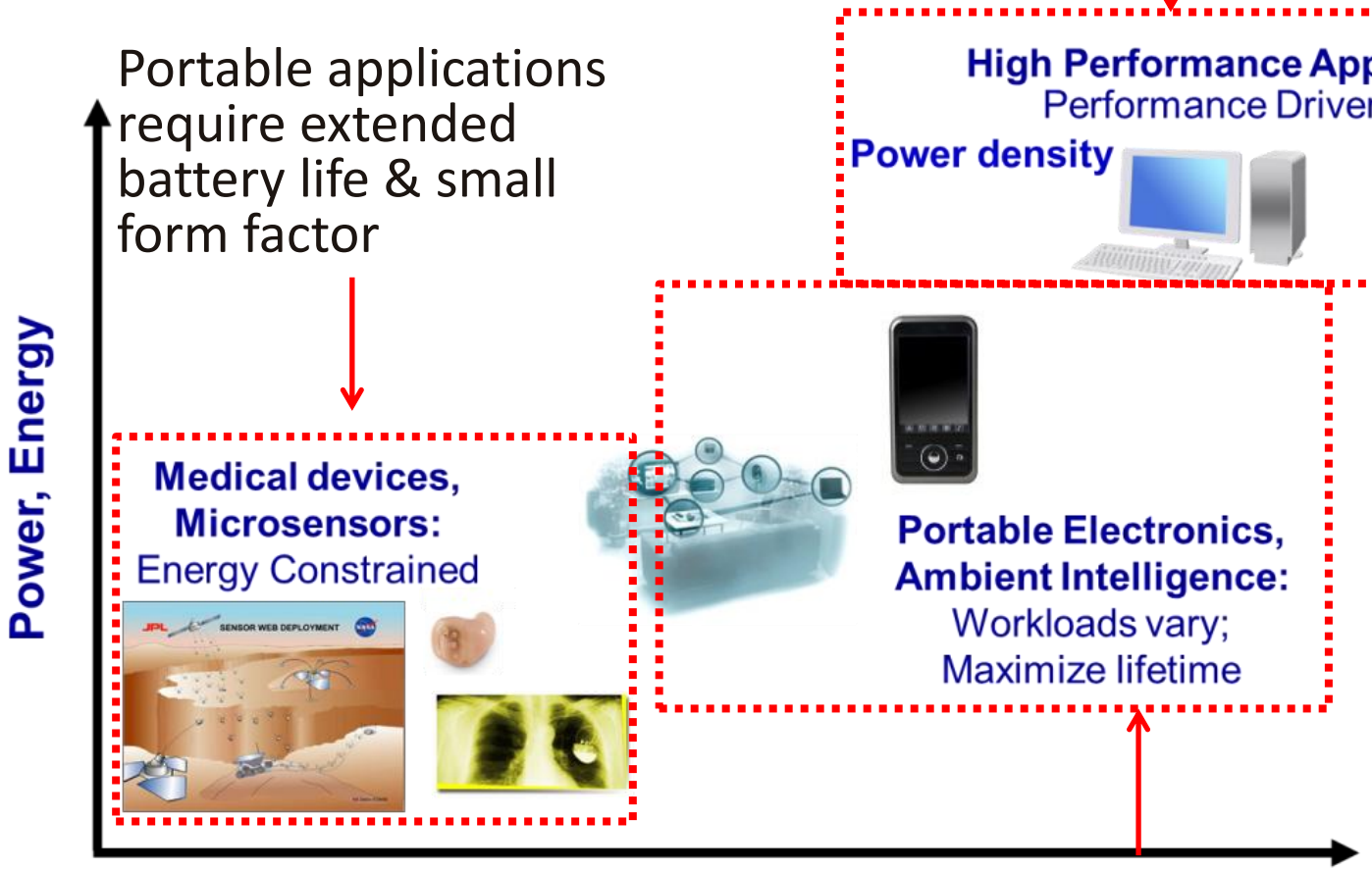
July 18, 2012

Robust Low Power VLSI

Motivation

High performance struggles with power density

Portable applications require extended battery life & small form factor



Electronics need high performance for a fraction of their life

Varying Conditions at Runtime

- Varying workload
  - Amount of data sampled/inputted
  - Mode change
- Varying amounts of harvest energy (in harvesting systems)
  - Temperature change
  - Cloudy day
  - Change in locations

How do we maximize functionality and reduce energy to account for these runtime variations to ensure a long lifetime?

Varying Workload

- Occasionally requires high performance.

→Panoptic Dynamic Voltage Scaling (PDVS) allows the system to adapt to varying normalized workloads from ~0 to 1.

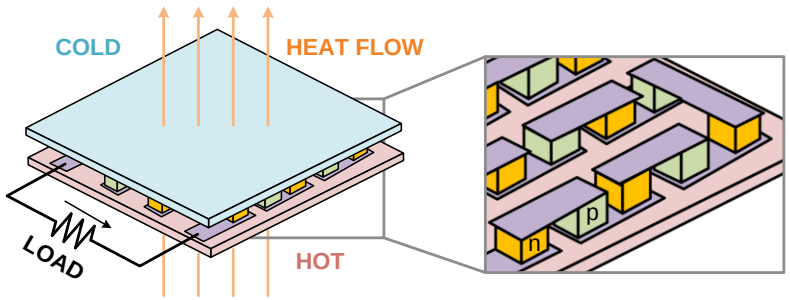
www.apple.com

Varying Amounts of Harvested Energy

- Harvesting energy - indefinite electronics lifetime and small form factor.
- 10's of µWs and highly environment-dependent.
- Nodes must consume low power (<~40µW)

→Architecture and power management is instrumental in achieving low power consumption.

Thermal Electric Generator



Zhang et al. *ISSCC 2012*

Proposed Thesis Contributions

1. Implementation of PDVS on a processor
2. An evaluation of system level savings and overheads of PDVS at varying workloads
3. A low power, state of the art Body Sensor Network node capable of running solely off harvested energy
4. An evaluation of power management policies
5. An energy harvesting-specific power management system capable of responding to changes in the amount of energy harvested

Outline

- **Responding to Dynamic Workloads**
  - **Panoptic Dynamic Voltage Scaling**
- Responding to Varying Energy Harvesting
  - Body Sensor Node Architecture
  - Energy Harvesting Specific Power Management
- Schedule

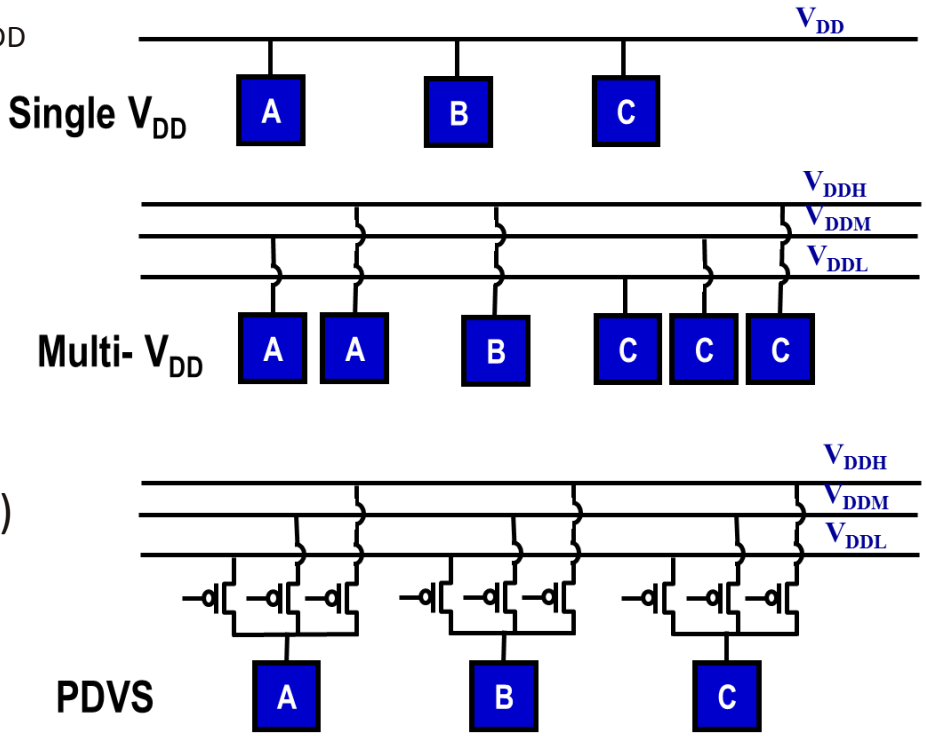
Motivation

- Occasionally requires high performance.
- Varying workload performance
- Designing in a static fashion → Shorter battery life

www.hp.com
www.nokia.com

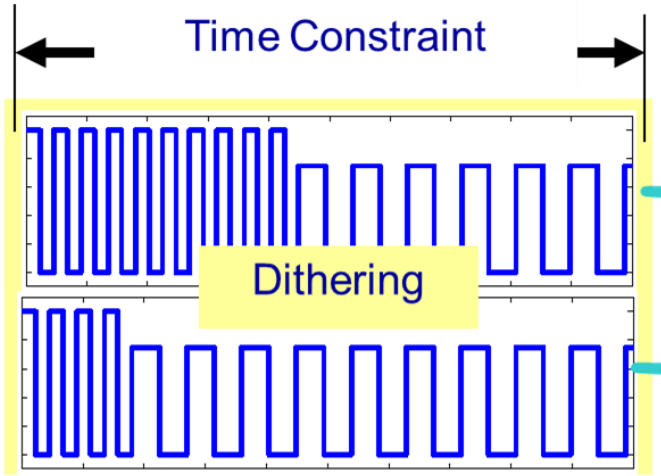
Panoptic DVS (PDVS) Structure

- Single-V_{DD}
  - All components share one V_{DD}
- Multi-V_{DD}
  - Each component statically tied to a V_{DD}
- PDVS
  - PMOS header switches used to select a specific V_{DD}
  - Small set of voltage rails (2-4)
  - Uses common components
  - Fine temporal granularity
  - Fine spatial granularity

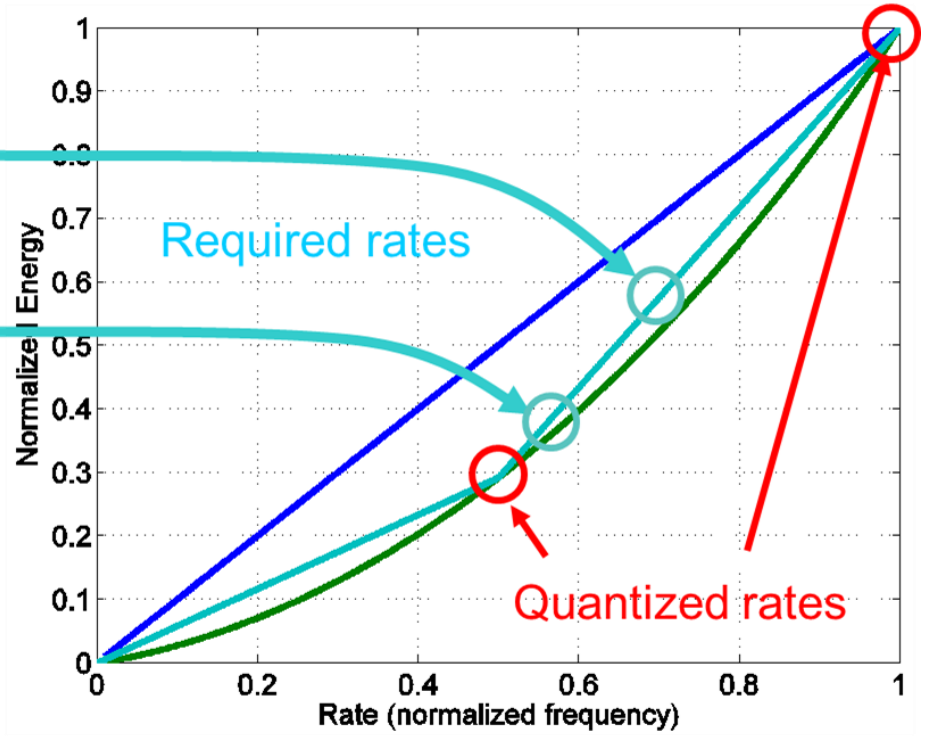


[1] Putic, M. et al., *ICCD*, pp.491-497, 01/10/2009.
[2] Di, L. et al., *ICCD,* pp.605-611, 08/2008.

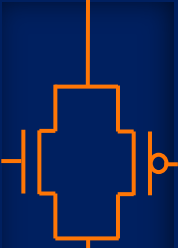
Dithering



Single VDD
Ideal DVS
Multi-V_{DD}/PDVS



[Gutnik, *SympVLSI*'96]

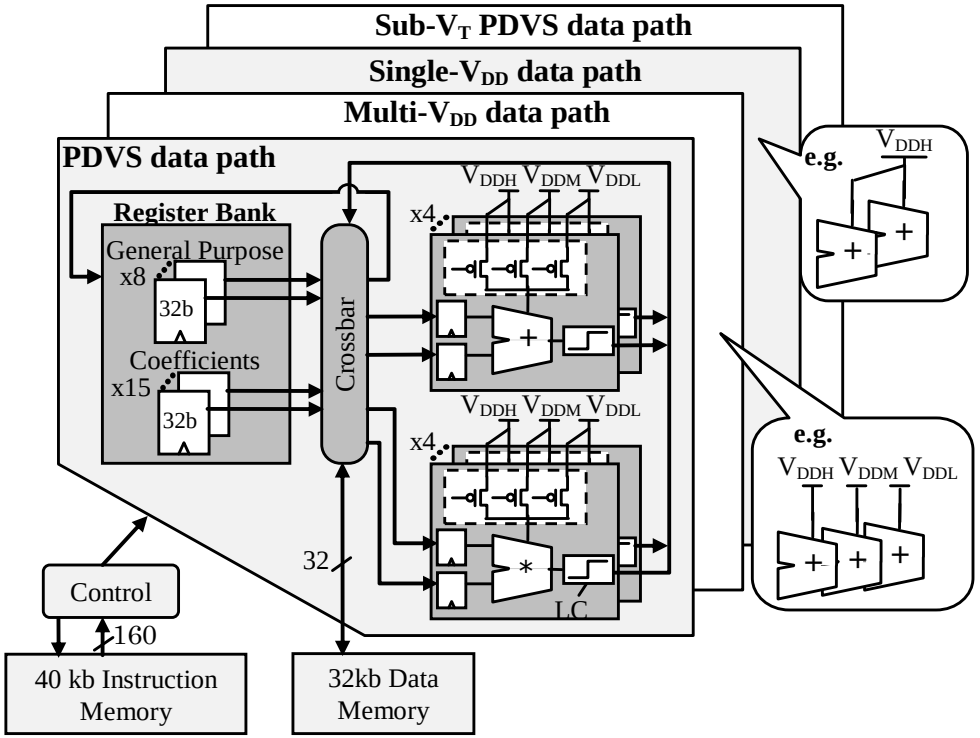


Hypothesis

Application of fine grained DVS using the **PDVS** scheme will result in **higher energy savings** on a system level **compared to single-V_{DD} and multi-V_{DD} alternatives**, despite the overheads of the scheme.

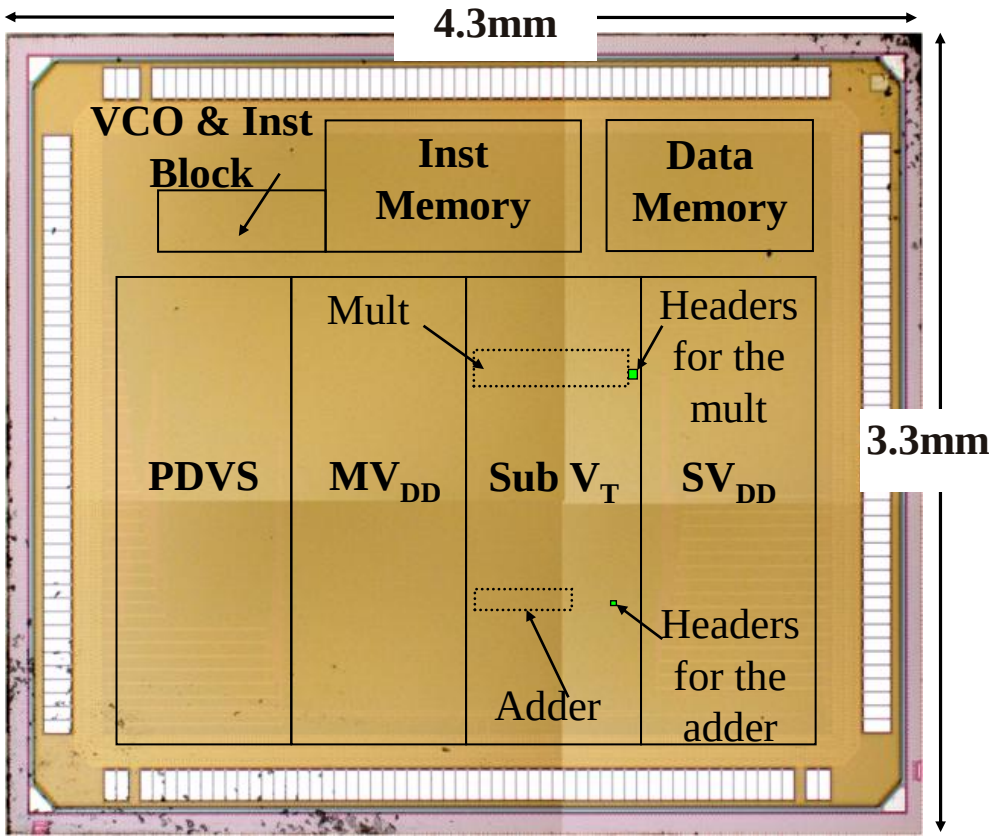
Approach

- 32b Data Flow Processor
  - 4 Kogge Stone Adders
  - 4 Baugh Wooley Multipliers
  - PMOS Header
  - Level Converters
- Execute arbitrary programs
- Four architectures for comparison

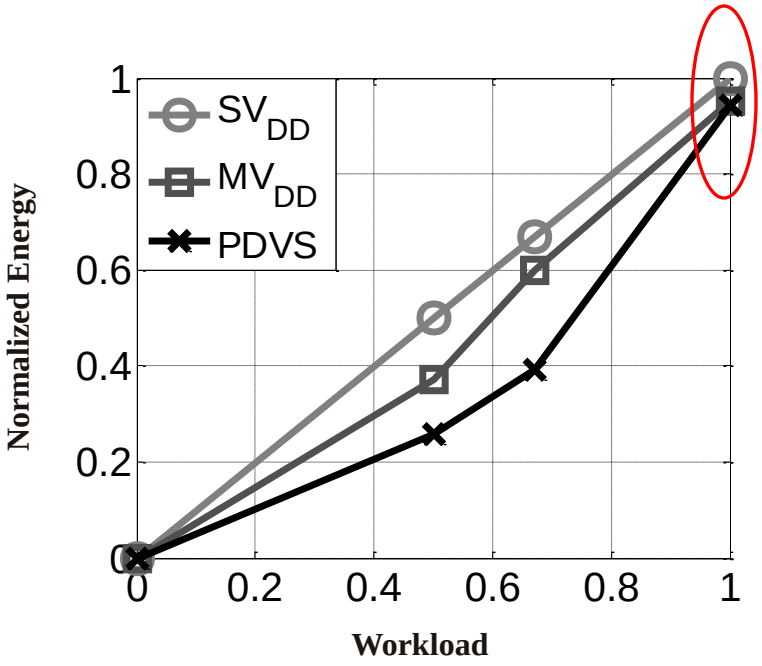


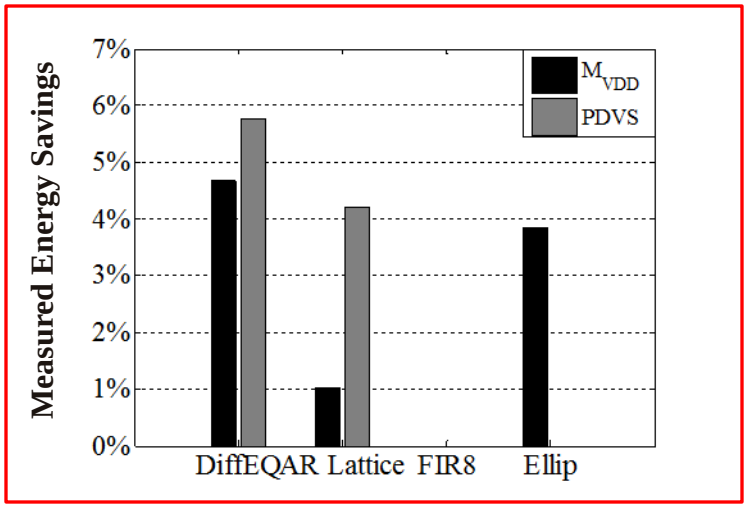
Test Chip

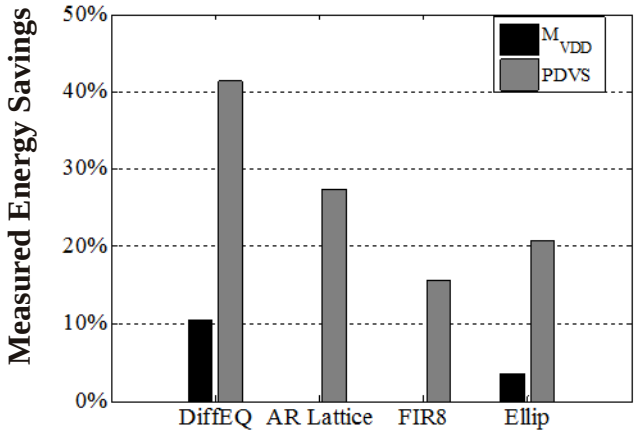
Feature	This Chip
Process	90nm CMOS Bulk w/ Dual V_T
Area	4.3mm x 3.3mm
Transistor Count	~2 million
V_{DD}	250mV – 1.2V
SRAMs	40kb & 32kb



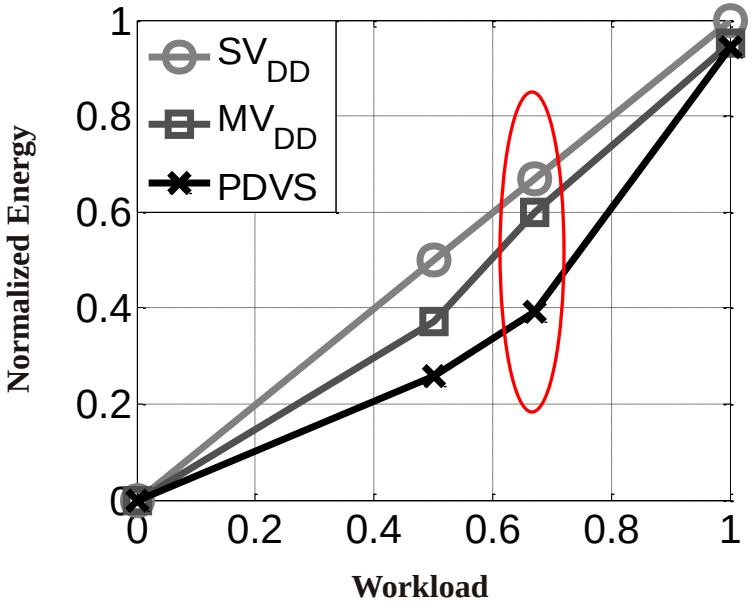
System Results

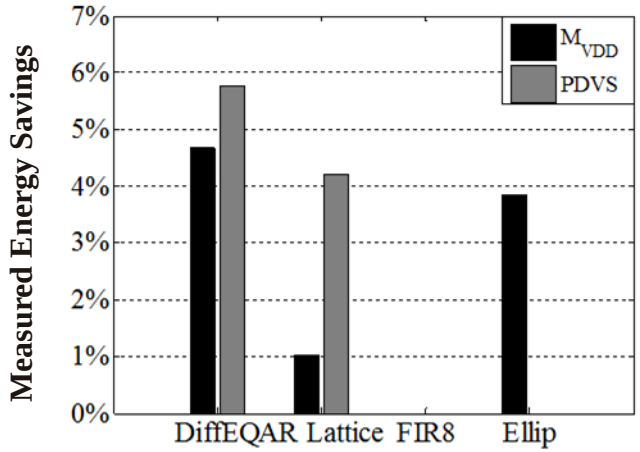


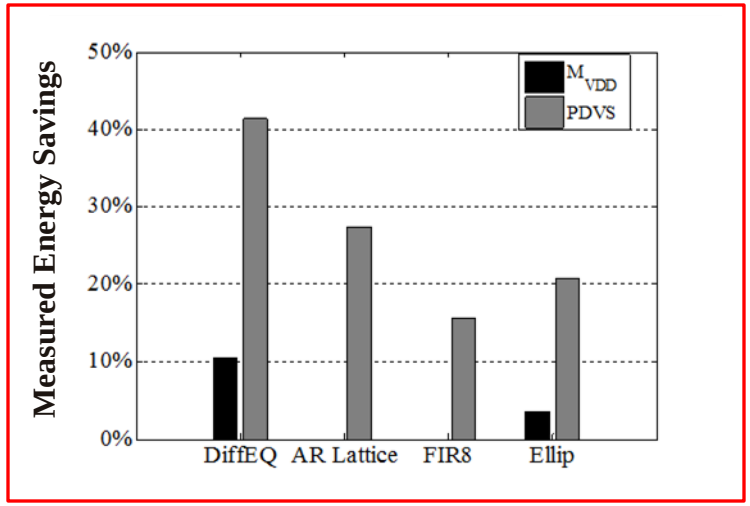




System Results Cont'd







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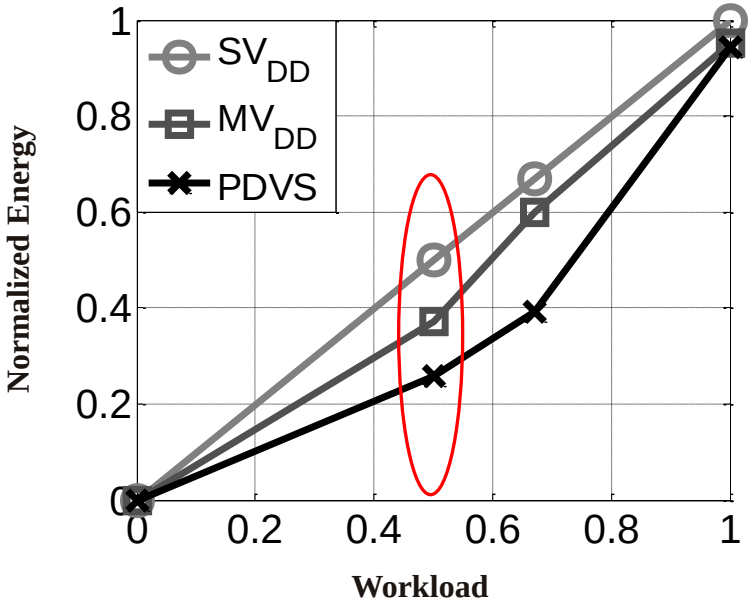
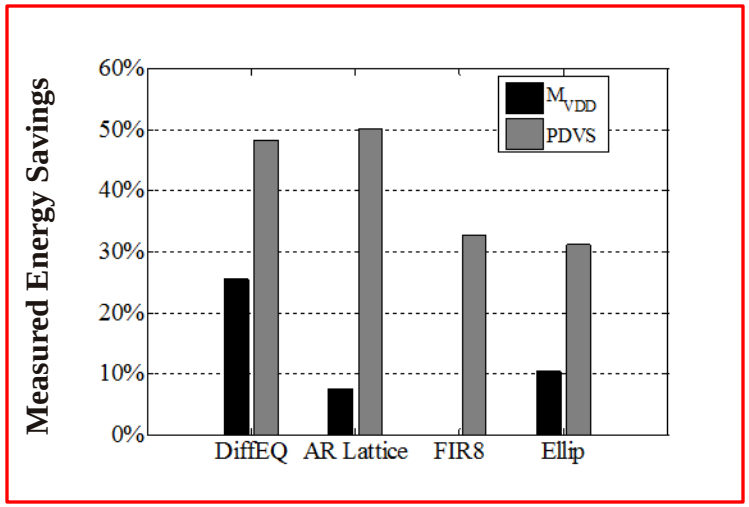
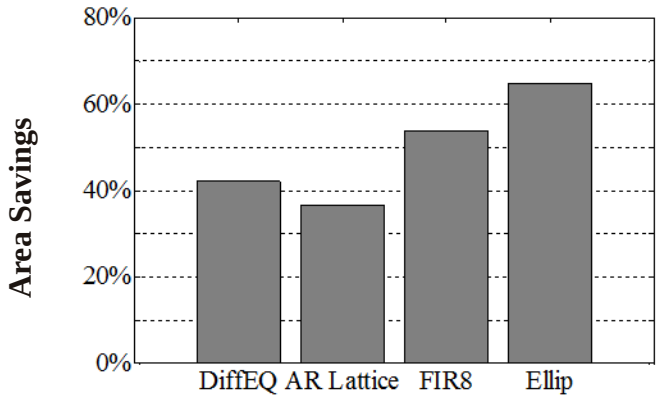
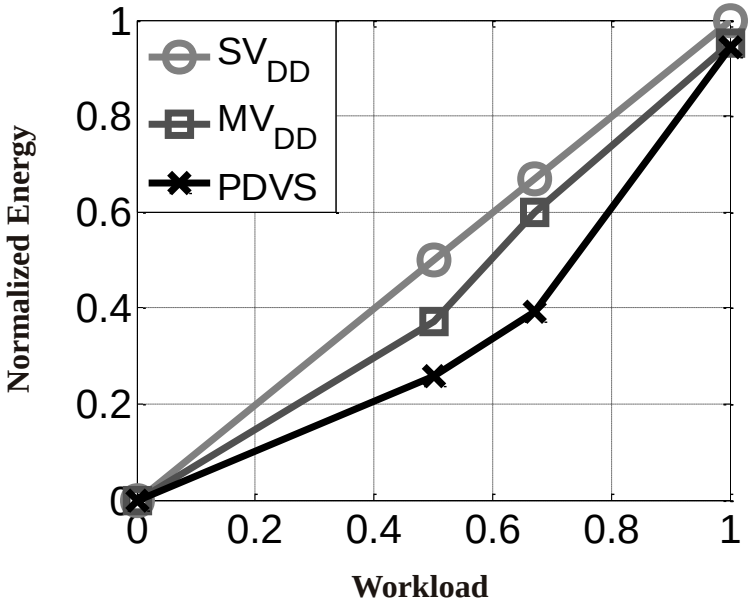


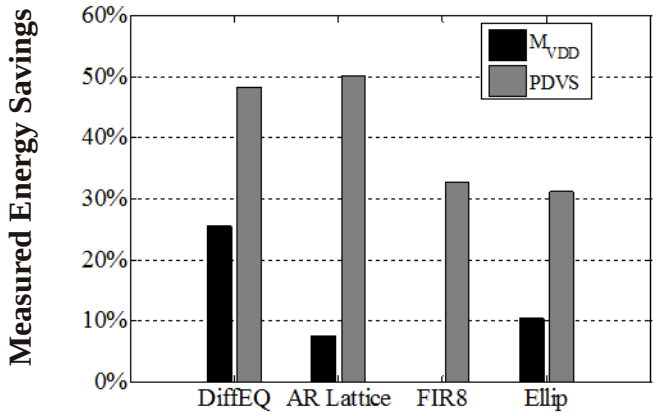
Introducing slack increases savings

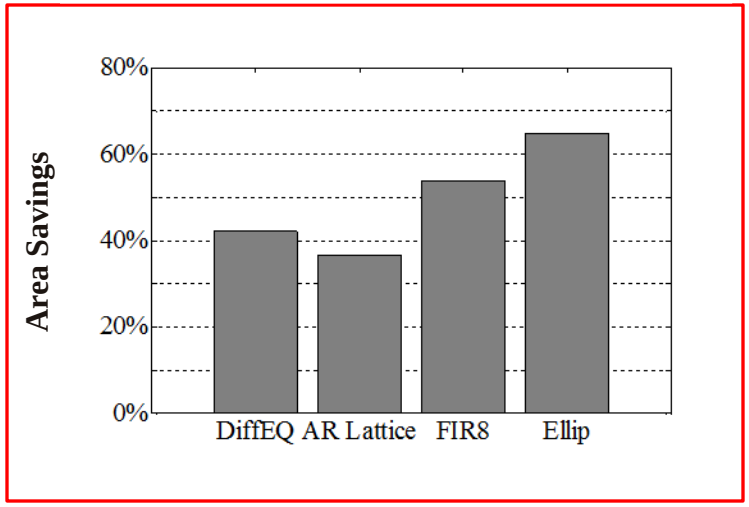




Area Savings vs Multi-V_{DD}





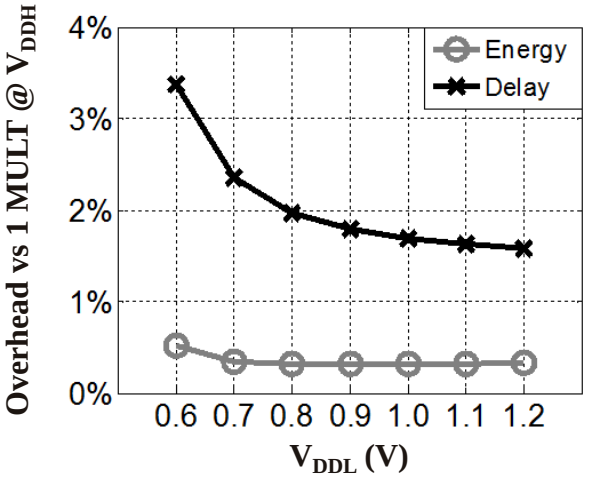


PDVS area savings are a result of reducing the number of copies

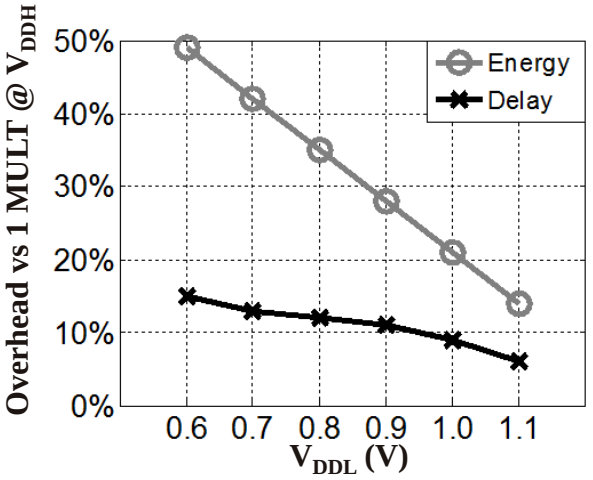
Overheads

	32b Adder	32b Mult.
Header Area	2.4%	1.7%
Level Conv. Delay	32.0%	2.0%
Level Conv. Energy	8.0%	0.3%
Level Conv. Area	11.4%	2.1%
Sw. Delay	10.4%	12.0%
Sw. Energy	215.3%	35.0%
Breakeven Cycles (N_{BE})	< 4	< 1

Multiplier level converter



Multiplier switching



PDVS Contributions

1. Demonstrated data flow processor using PDVS in silicon
2. Demonstrated single clock cycle V_{DD}-switching & V_{DD} dithering for near optimal energy scalability
3. Demonstrated energy savings compared to single-V_{DD} and multi-V_{DD} alternatives.

Feature	*Howard ISSCC10*	*Truong VLSI08*	*Nam ISSCC07*	*This work*
V_{DD} Granularity	6 cores	1 core	1 core	Add, Mult
Speed of V_{DD} change	>10µs (e.g.[4])	2-5ns	>10µs (e.g. [4])	<2ns
V_{DD} dithering	No	No	No	Yes
Sub-threshold	No	No	No	Yes

[1] J. Howard et al., *ISSCC* , pp. 22-33, 2010.
[2] D. Truong et al., *Symp. VLSI,* pp.22-23, 2008.
[3] B. Nam et al., *ISSCC*, pp.278-603, 2007.
[4] C. Zheng and D. Ma, *ISSCC*, pp.204-205, 2010.

Publications

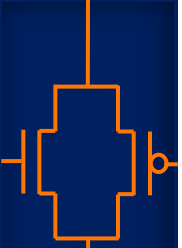
1. B. H. Calhoun, S. Arrabi, S. Khanna, Y. Shakhsheer, K. Craig, J. Ryan, and J. Lach. “REESES: Rapid Efficient Energy Scalable ElectronicS.” *GOMACTech*. March 2010.

2. S. Khanna, K. Craig, Y. Shakhsheer, S. Arrabi, J. Lach, and B. H. Calhoun. “Stepped Supply Voltage Switching for Energy Constrained Systems.” *ISQED*. March 2011.

3. Y. Shakhsheer, S. Khanna, K. Craig, S. Arrabi, J. Lach, and B. H. Calhoun, "A 90nm Data Flow Processor Demonstrating Fine Grained DVS for Energy Efficient Operation from 0.25V to 1.2V", *CICC*, September 2011.

4. K. Craig, Y. Shakhsheer, and B. H. Calhoun. "Optimal Power Switch Design for Dynamic Voltage Scaling from High Performance to Subthreshold Operation", *ISLPED* , July 2012.

5. K. Craig, Y. Shakhsheer, S. Khanna, S. Arrabi, J. Lach, B. H. Calhoun, and S. Kosonocky, "A Programmable Resistive Power Grid for Post-Fabrication Flexibility and Energy Tradeoffs", *ISLPED*, July 2012.



Outline

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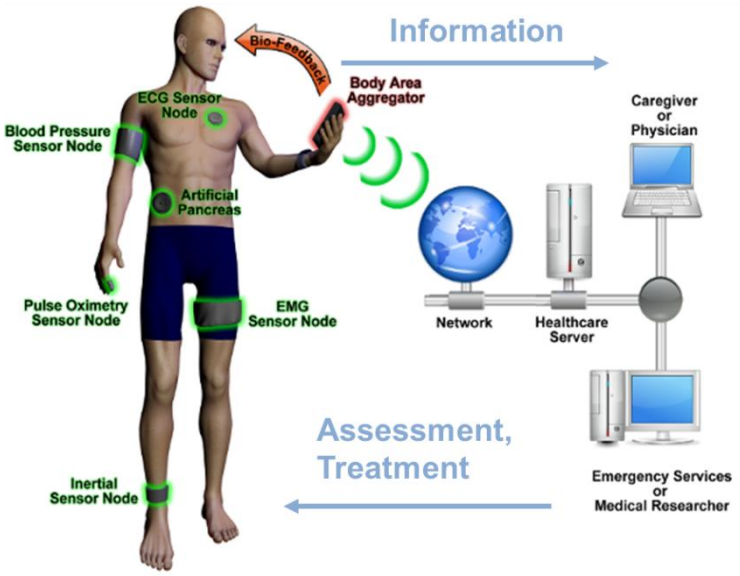
- **Responding to Varying Energy Harvesting**
  - **Body Sensor Node Architecture**
  - Energy Harvesting Specific Power Management
- Schedule

Body Sensor Network Nodes



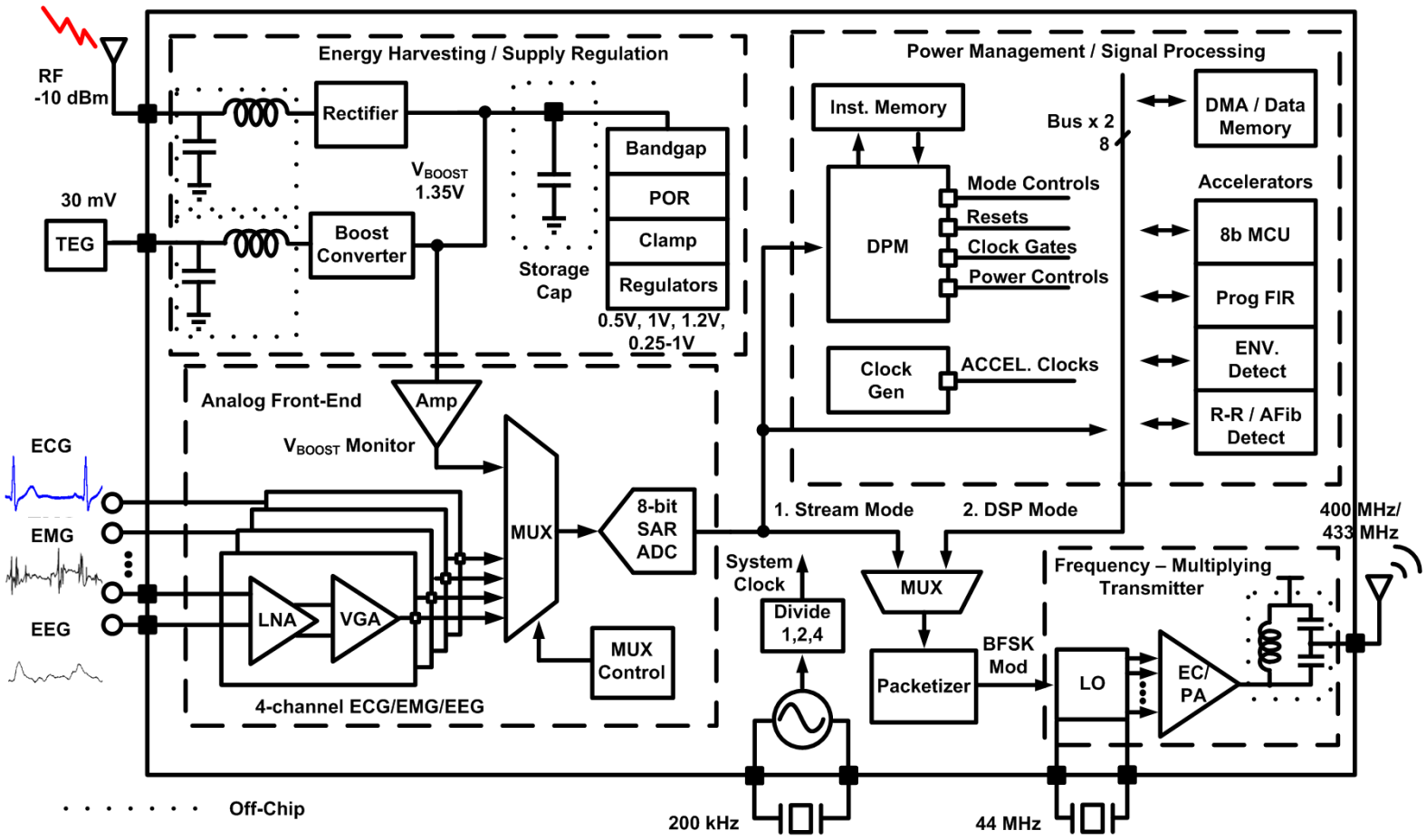
Compliance requirements:

- Long lifetime
- Small form factor for wearability
- Low cost

Hypothesis

A BSN node **utilizing a low power microcontroller, low power accelerators, a low power analog front end, and a low power transmitter** with intelligent duty cycling will be capable of running **solely off harvested energy.**

System Block Diagram



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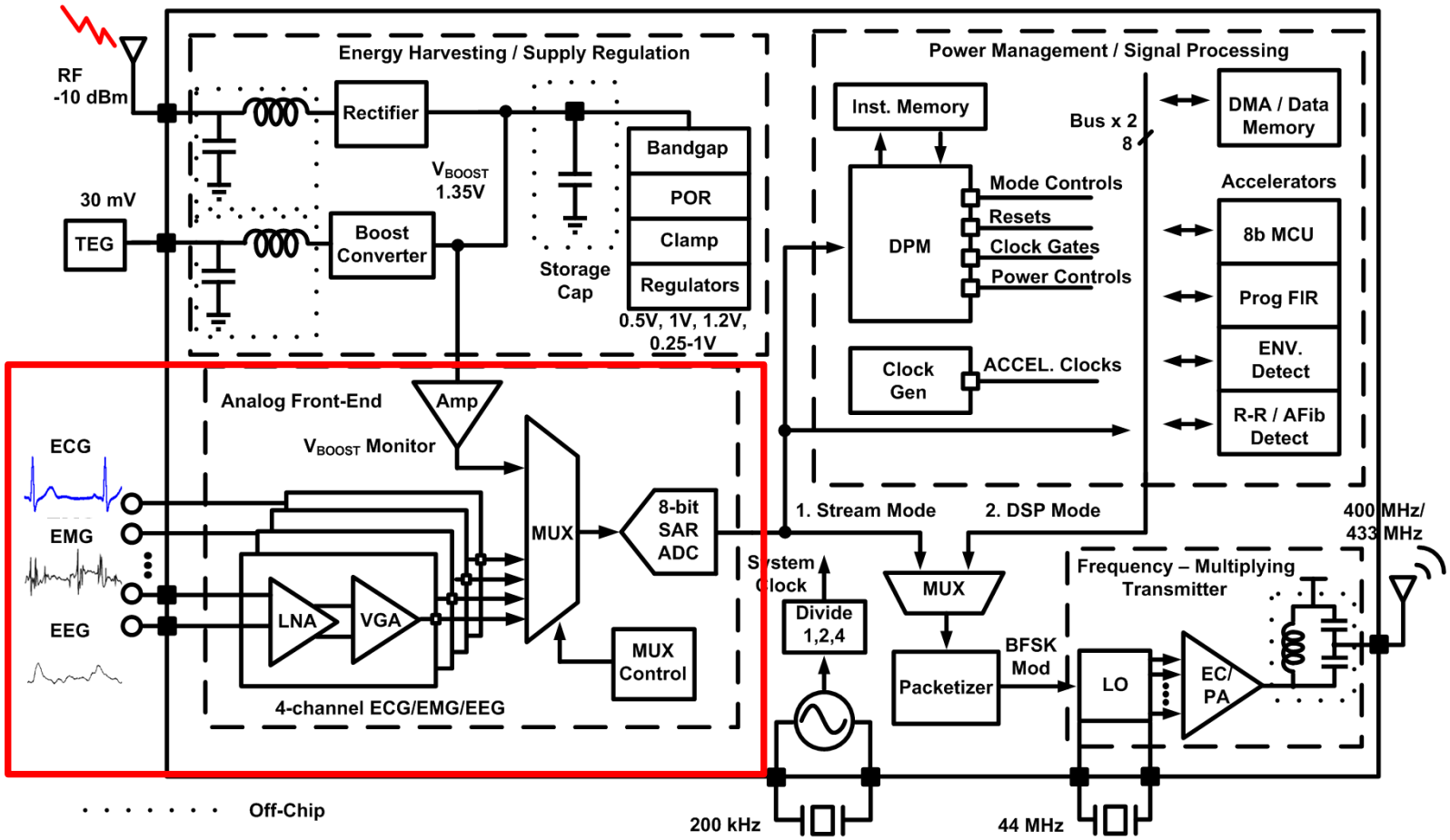

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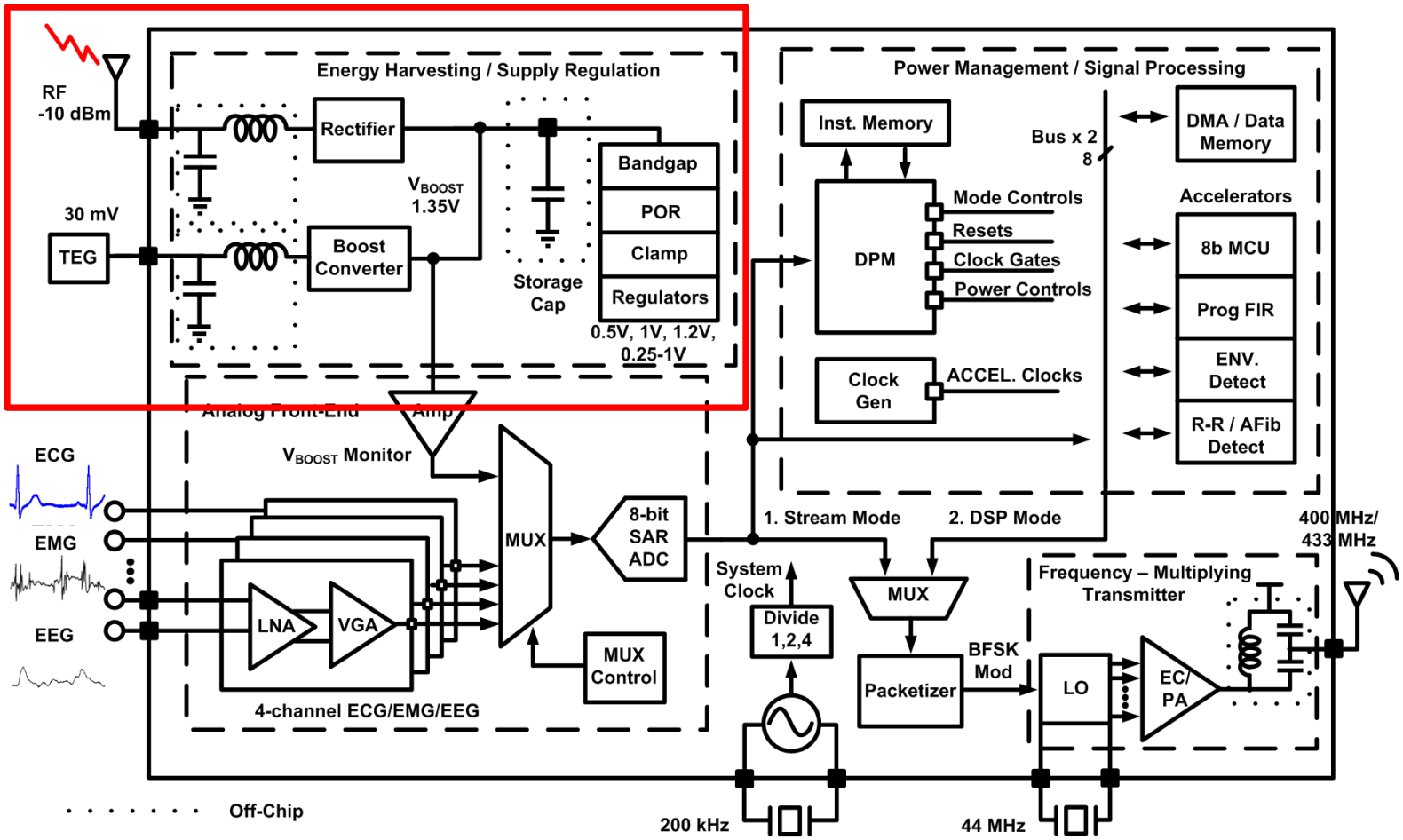

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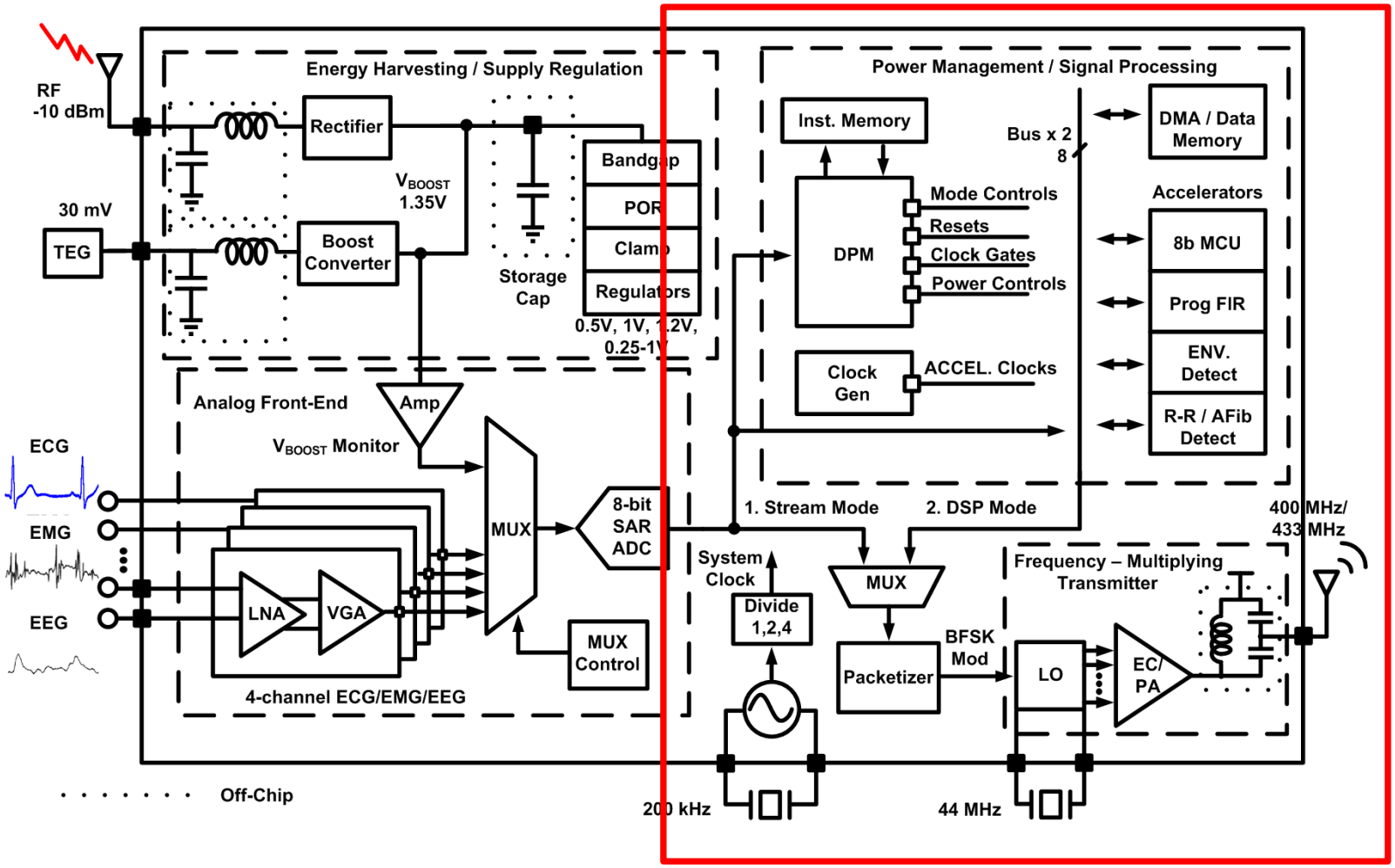
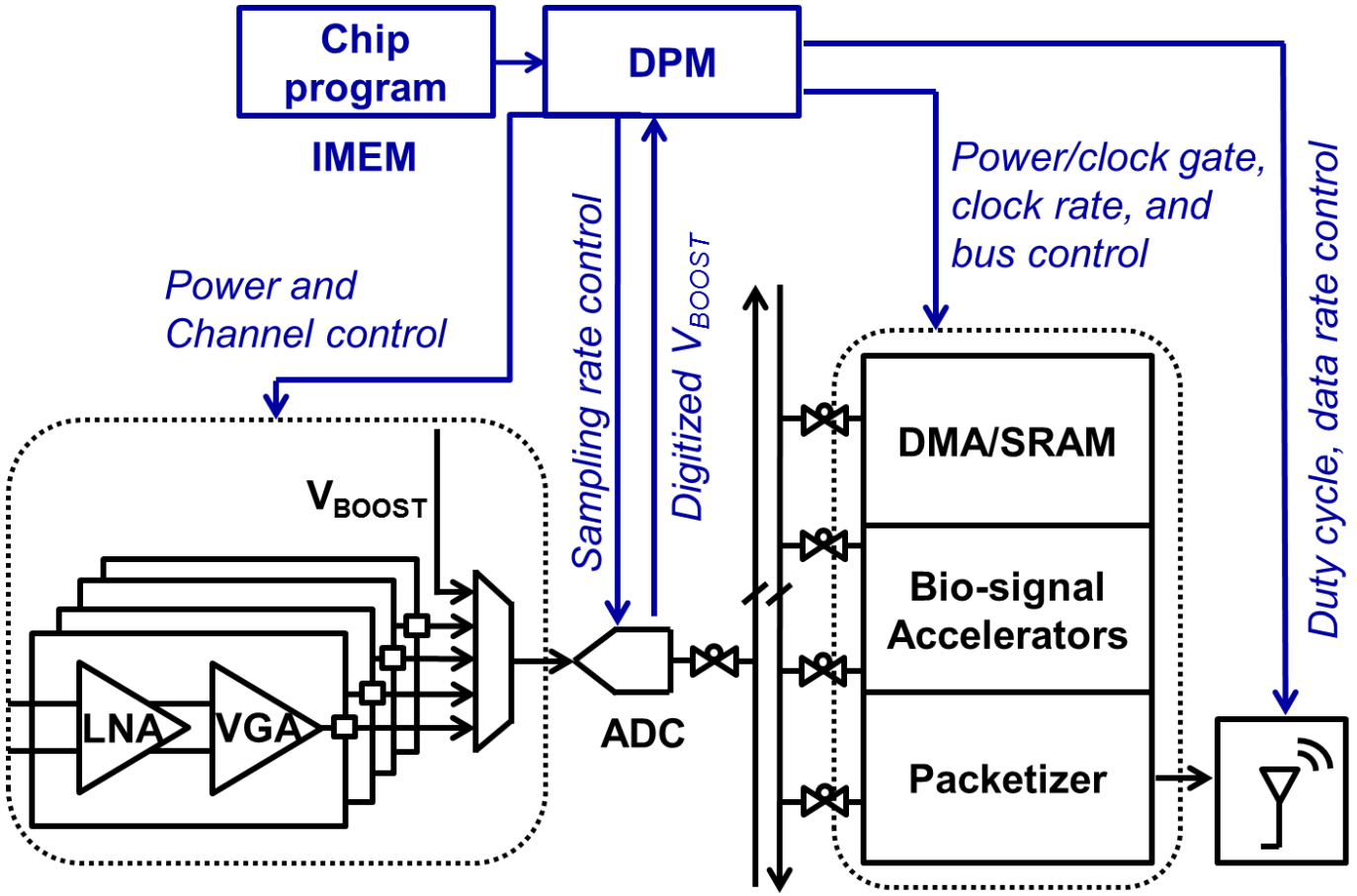
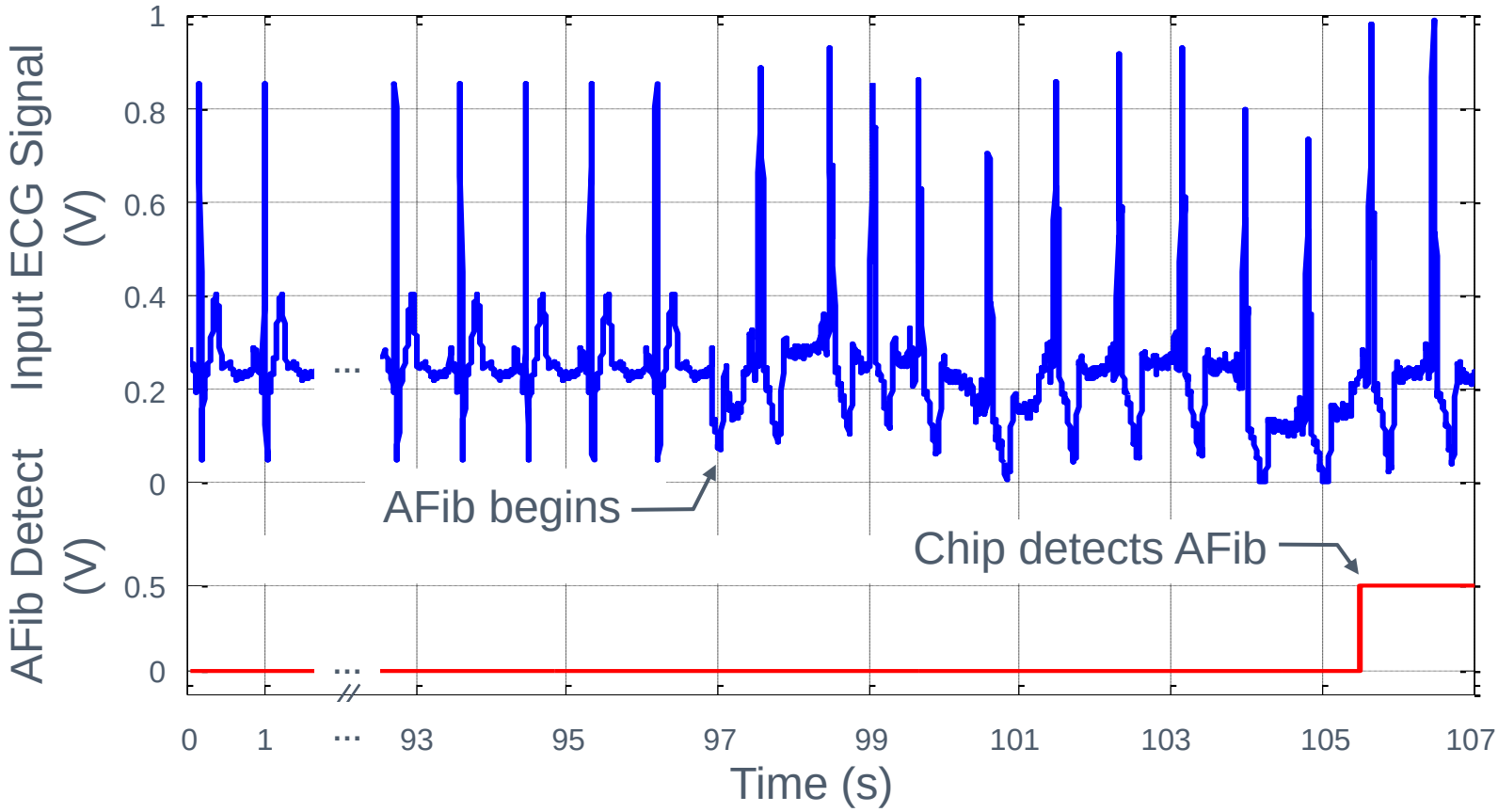


Digital Power Manager



Results



- When a rare AFib occurs, TX is enabled to transmit the last 8 beats of ECG (in the data memory).
- 19 µW from V_{BOOST}
- Powered from a 30mV input

SoC Ultra-Low PoweR (SUPR) Model

Need the ability to model BSN nodes for hardware selection

SUPR provides this opportunity

Improvements include:

- Expanding on # of experiments
- Improvements to the power harvesting/management simulation

Proposed Architecture Contributions

- A low power, state of the art BSN node capable of running solely off harvested energy
- A low power, custom MCU responsible for power management, node control, data flow management, and overseeing all processing on the battery-less BSN node more efficiently than a generic MCU
- Improvements to the SoC Ultra-Low PoweR (SUPR) Model for modeling BSN nodes

Publications

1. Y. Shakhsheer, Y. Zhang, B. Otis, and B. H. Calhoun, "A Custom Processor for Node and Power Management of a Battery-less Body Sensor Node in 130nm CMOS", *CICC*, September 2012.

2. F. Zhang, Y. Zhang, J. Silver, Y. Shakhsheer, M. Nagaraju, A. Klinefelter, J. Pandey, J. Boley, E. Carlson, A. Shrivastava, et al., "A Batteryless 19uW MICS/ISM-Band Energy Harvesting Body Area Sensor Node SoC", *ISSCC*, 02/2012.

3. Y. Zhang, Y. Shakhsheer, A. T. Barth, H. P. C. Jr., S. A. Ridenour, M. A. Hanson, J. Lach, and B. H. Calhoun, "Energy Efficient Design for Body Sensor Nodes", *Journal of Low Power Electronics and Applications*, April 2011.

4. B. H. Calhoun, Y. Zhang, S. Khanna, K. Craig, Y. Shakhsheer, J. Lach. "A Sub-Threshold FPGA: Energy-Efficient Reconfigurable Logic."*GOMACTech*. March 2011.

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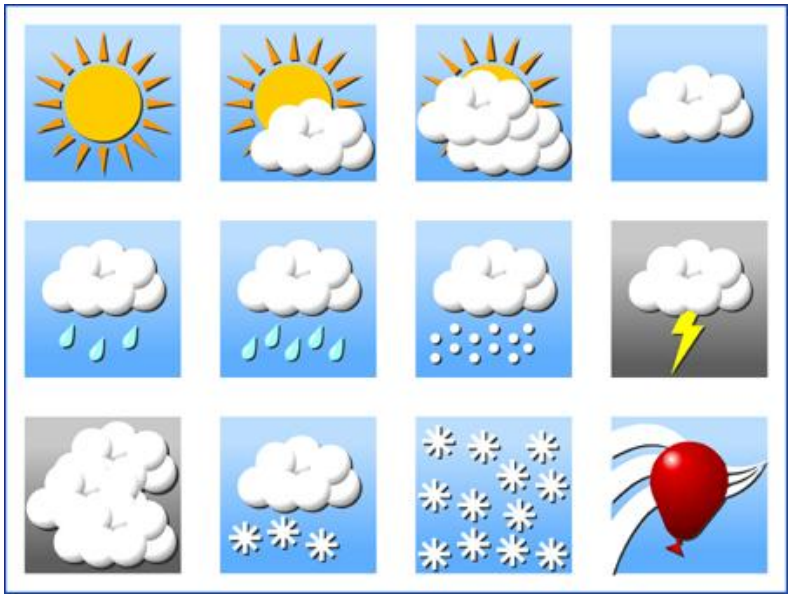
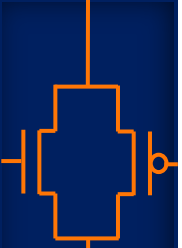
Energy Harvesting Challenges

- High peak current
- High power operations exceed the power budget
- Power harvester highly environment-dependent.

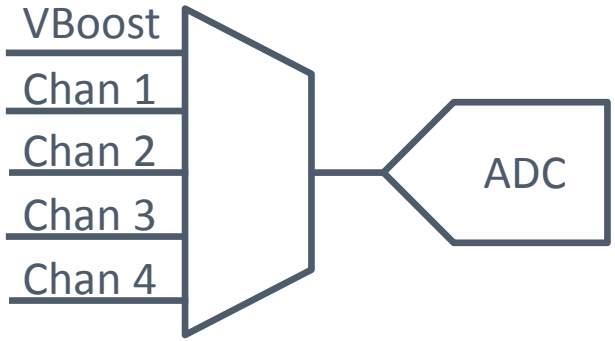




Hypothesis

A closed loop, **energy harvesting-specific stoplight power management, capable of single-cycle power consumption adjustment, will result in longer node lifetime and more robust energy harvesting node.** Adding simple hardware to predict the harvesting rate and asymmetric operating mode thresholds will result in a longer node lifetime despite its overheads.

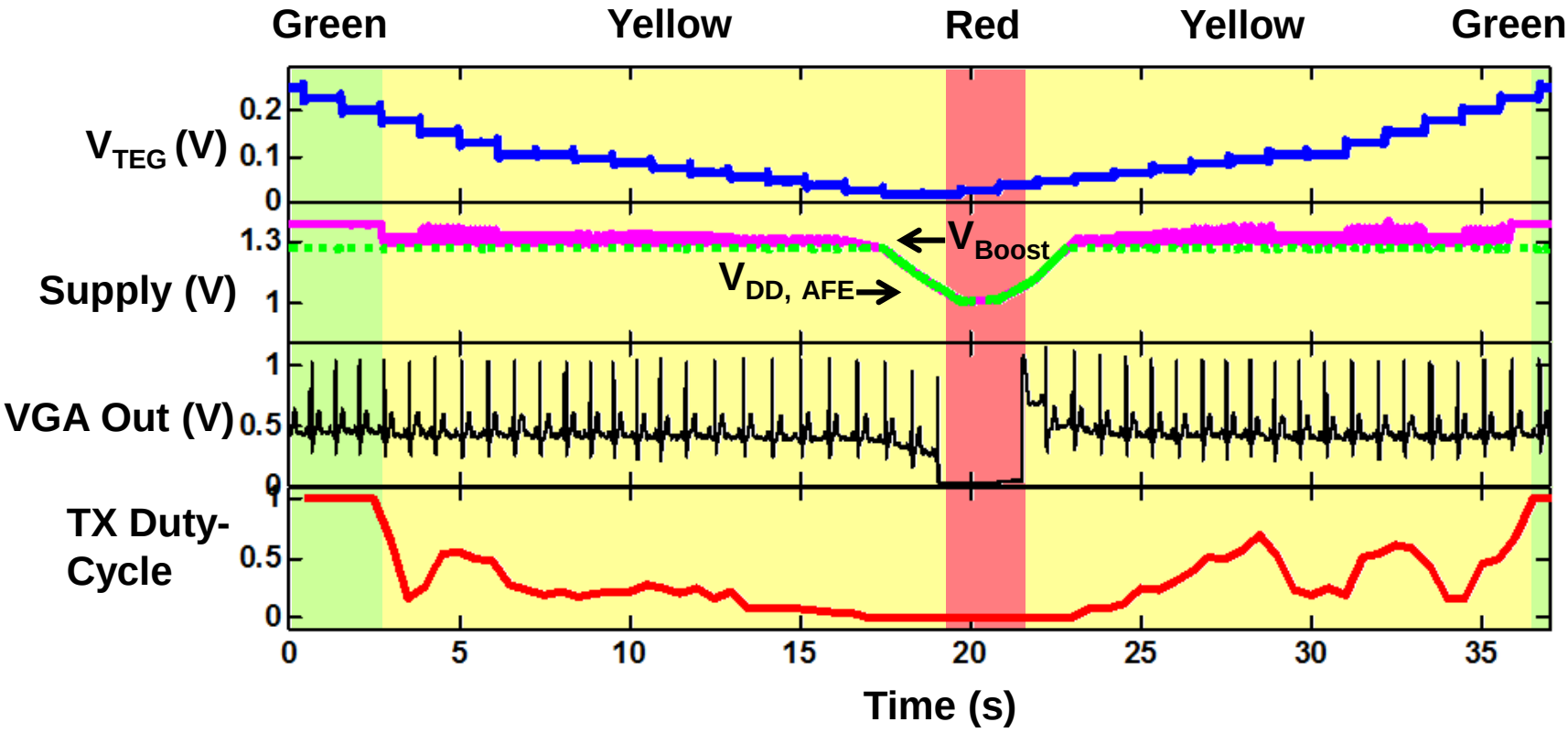
Approach: Revision 1



Mode	Green	Yellow	Red
Threshold	PROG	PROG	PROG
Transmit	✓	✓/✗	✗
Process	✓	✗	✗
Data Mem	✓	✓	✗
Inst Mem	✓	✓	✓

- Ability to program thresholds to needs
- Ability to constrain operations as needed through subroutines

Results: Revision 1



Approach: Revision 2

- Goal: To provide a more flexible, scalable, robust power manager
- Explore knobs
  - Checking energy on the storage capacitor
  - Prediction
  - Asymmetric thresholds
  - Programmable operating modes

Proposed Contributions

1. The first implemented energy-harvesting specific power management system of an energy harvesting node

2. A flexible, energy efficient power manager capable of being used on multiple energy harvesting nodes.

Publications

1. Y. Shakhsheer, Y. Zhang, B. Otis, and B. H. Calhoun, "A Custom Processor for Node and Power Management of a Battery-less Body Sensor Node in 130nm CMOS", *CICC*, September 2012. (Accepted for publication)

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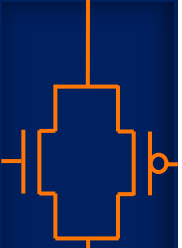

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Schedule

Subject	#	Task Description	Status/Target	Pubs
PDVS	1	Design Exploration	Done	
	2	Simulations	Done	
	3	Schematic/Layout	Done	[YAS1]
	4	Test Chip	Aug 2012	[YAS3] [YAS4][YAS7][YAS9] [YAS10][YAS13]
BSN Architecture	1	Design Exploration	Done	[YAS5]
	2	RTL	Done	
	3	Synthesis	Done	
	4	Test Chip	Done	[YAS8] [YAS11] [YAS12]
	5	Work with SUPR Model	Nov 2012	[YAS14]
Power Management	1	Rev 1: Design Exploration	Done	
	2	Rev 1: RTL	Done	
	3	Rev 1: Synthesis	Done	
	4	Rev 1: Test Chip	Done	[YAS11]
	5	Rev 2: Design Exploration	Sept 2012	
	6	Rev 2: RTL	Oct 2012	
	7	Rev 2: Synthesis	Nov 2012	
	8	Rev 2: Test chip	Sept 2013	[YAS15]
Write Up	1	Thesis Writing	Nov 2013	

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- **Y. Shakhsheer**, Y. Zhang, B. Otis, and B. H. Calhoun, "A Custom Processor for Node and Power Management of a Battery-less Body Sensor Node in 130nm CMOS", *CICC*, September 2012. (Accepted for publication)
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- K. Craig, **Y. Shakhsheer**, S. Khanna, S. Arrabi, J. Lach, B. H. Calhoun, and S. Kosonocky, "A Programmable Resistive Power Grid for Post-Fabrication Flexibility and Energy Tradeoffs", *ISLPED*, July 2012.
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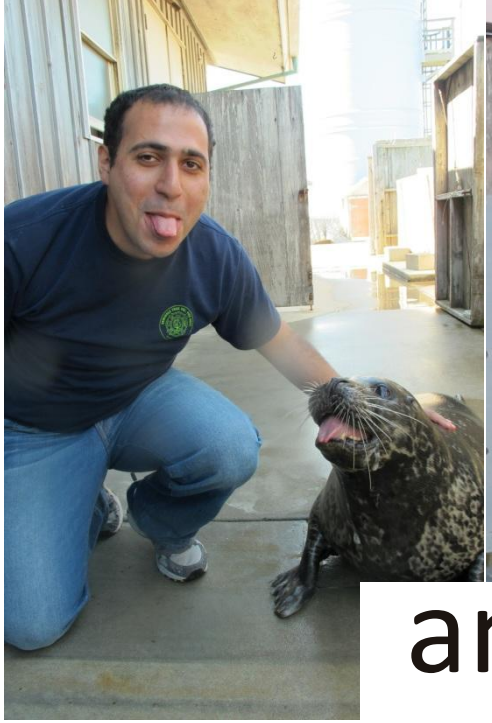
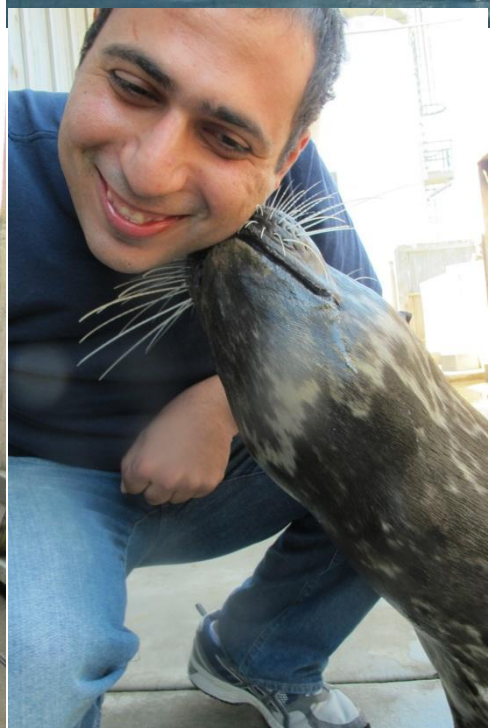
Thank you

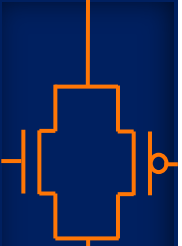
- The committee:
  - Dr. Mircea Stan
  - Dr. John Lach
  - Dr. Harry Powell
  - Dr. Kevin Skadron
- My advisor: Dr. Ben Calhoun
- RLPVLSI (aka BenGroup): Jiajing, Randy, Satya, Sudhanshu, Joe, Kyle, YQ, Alicia, Jim, Aatmesh, Craig, Seyi, and the newer students
- Fellow Grad Students: Stuart, Jonathan, Jeff, Ben B., Nate, the CPS group
- Friends and Family



and Sprouts

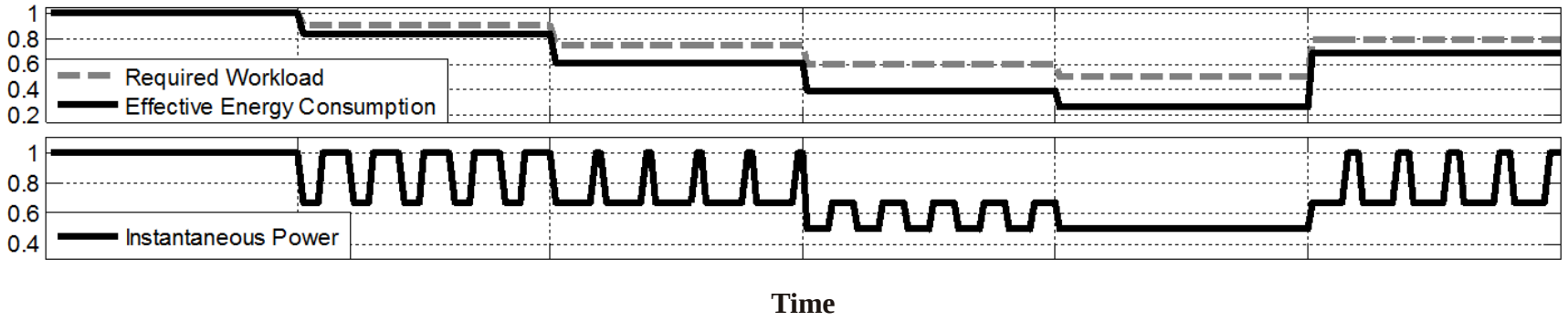
and friends.



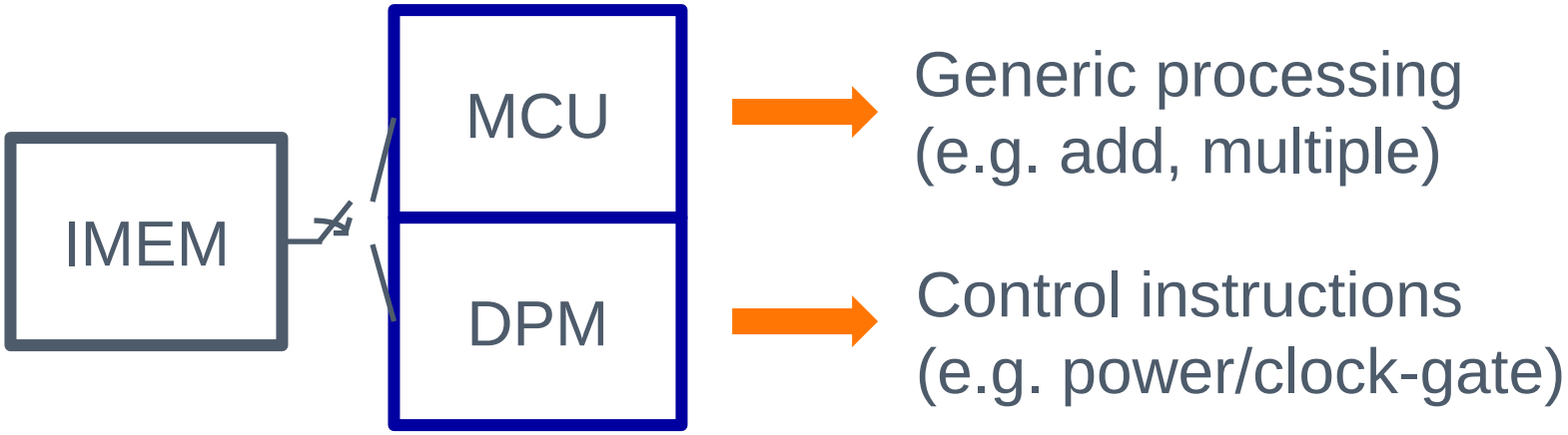


Back up slides

Measured Dithering



MCU vs DPM



- Execution of instructions toggles automatically between MCU and DPM.

Operation	DPM Energy	MCU Energy
NOP	0.7 pJ	1.46 pJ
Control Signals	2.8 pJ	2.92 pJ
Branch Commands	2.9 pJ	4.38 pJ

BASN Chip

	This Work	Kim VLSI'11	Rai ISSCC'09	Verma JSSC'10	Yan JSSC'11	Chen ISSCC'10
Micro-processor	1.5 pJ/Inst 200kHz (8b RISC ISA)	×	×	×	×	28.9 pJ/Inst 73kHz (32b COR-M3)
Accelerator	Prog. FIR, AFIB, DMA, Env. Det., Packetizer	4x SIMD, FIR, DMA, Encryption	×	ASIC DSP	FIR, Packetizer, Compression	×
Memory	5.5kB (0.3-0.7V)	42kB (1.2V)	×	×	20kB (1.2V)	5kB (0.4V)
Dig. Power	2.1µW	~12µW	N/A	2.1µW	500µW	2.1µW (MCU)
Total Power	19µW	31.1µW	500µW	77.1µW	2.4mW	7.7µW
Note on Total Power (includes):	8b ADC, DSP (R-R extract), TX at 0.013% DC	12b ADC, DSP (heart beat detection)	8b ADC, TX at 100% DC	12b ADC, DSP (EEG feature extraction)	10b ADC, DSP (data comp, FIR), SRAM, TX at 5% DC	Data acquisition, DSP (DFT), SRAM
Technology	130nm	180nm	130nm	180nm	180nm	180nm

Comparison with prior work (cont.)

	This Work	Kim VLSI'11	Rai ISSCC'09	Verma JSSC'10	Yan JSSC'11	Chen ISSCC'10
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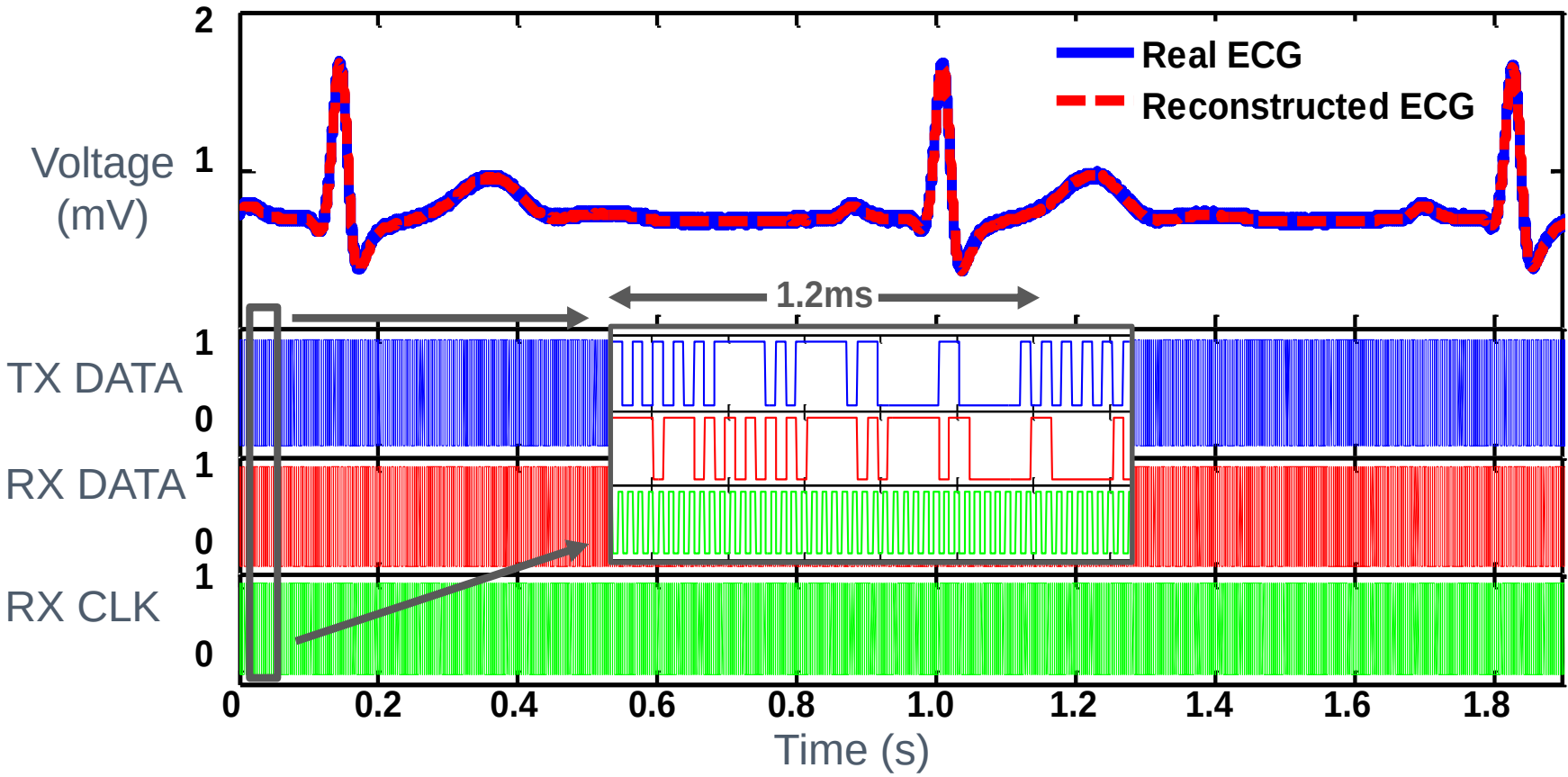
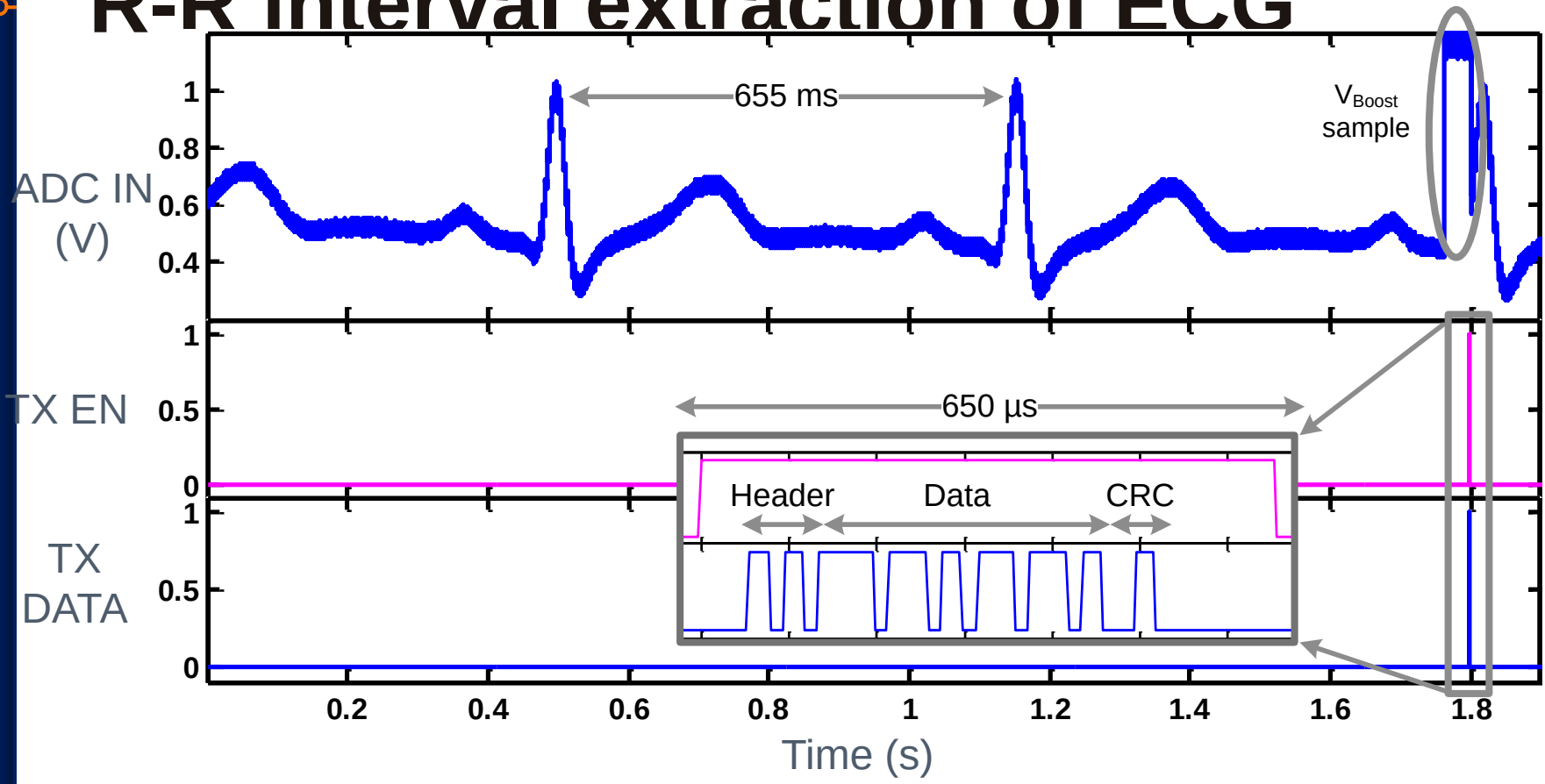
Continuous transmission of ECG



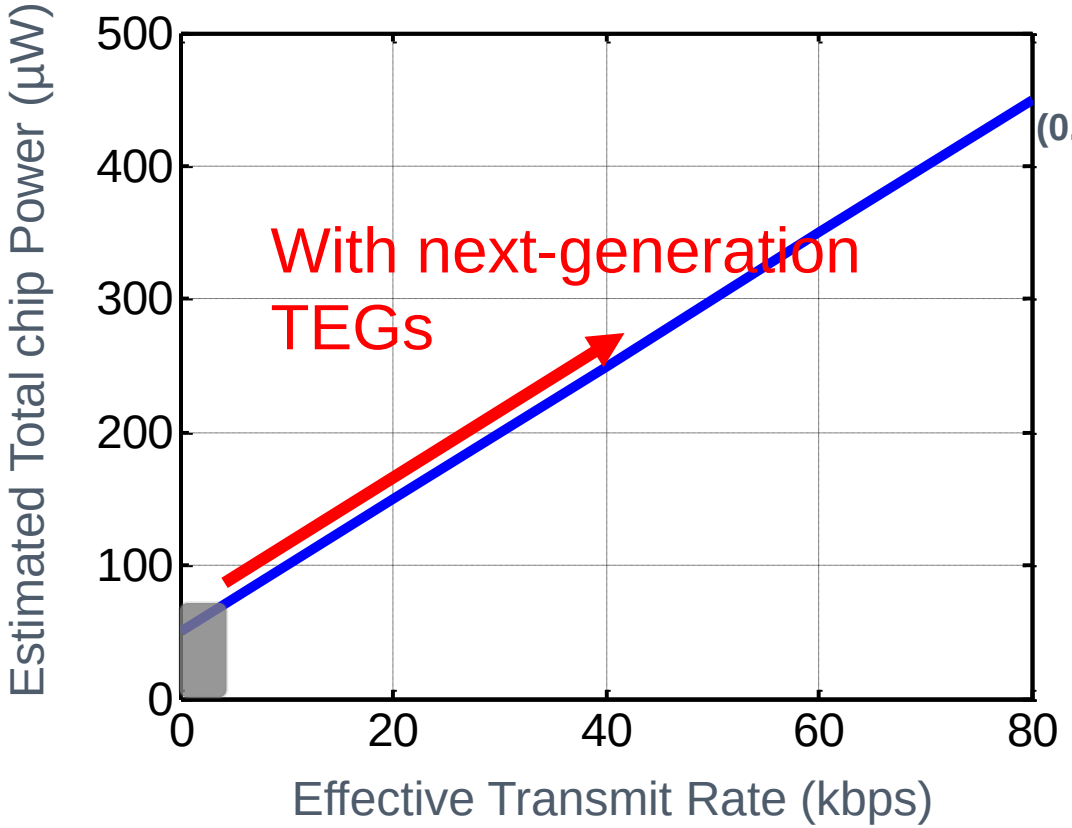
- ECG signal measured from a healthy human subject
- Wireless link demonstrated between the custom IC and commercial receiver (TI CC1101)
- 397 µW from V_{BOOST}

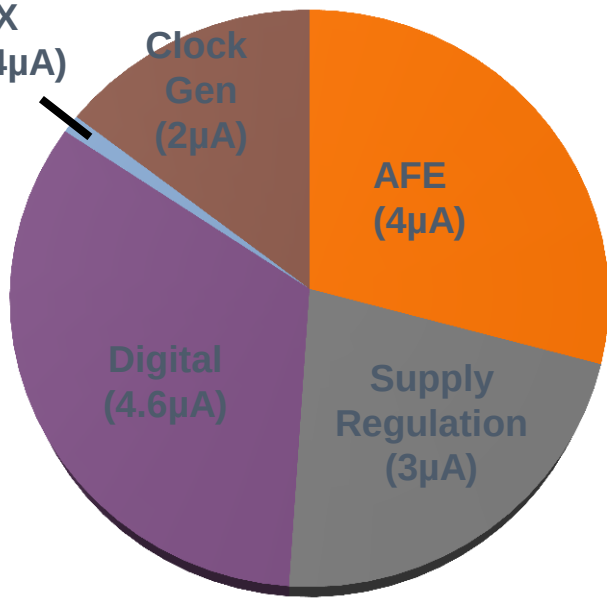
R-R interval extraction of ECG



- Every 5s, V_{BOOST} is sampled to check for sufficient energy
- DPM enables RF crystal oscillator (20ms) and TX (650µs)
- 19 µW from V_{BOOST}
- Powered from a 30mV input

Selective transmission





TX DC: 0.013%

Battery-free with TEGs today

- Selective TX and ULP circuits enable energy harvesting

SoC die photo

0.13 µm CMOS